20IT 402 Digital Electronics and Computer architecture

Flipped Classroom activity (2021-22, Sem - I)

04-Jan-2022

2021-22

Description: To implement the flipped classroom activity, the YouTube video link https://www.youtube.com/watch?v=3NXyTxo82CQ, was shared with the students in Google Classroom.

The video explained how 8086 works in Minimum mode of operation and how to draw timing diagrams for read and write cycle in Minimum mode. Students were asked to go through the video and learn the concept. Based on the understanding students were asked to try timing diagram for Maximum mode of 8086 too.

A doubt clearance session on Minimum and Maximum modes was conducted, in which the concept was again briefly discussed in class. After the discussion, to check the understanding of the concept, an assignment based on modes of operation for 8086 was uploaded in Google classroom which had following questions;

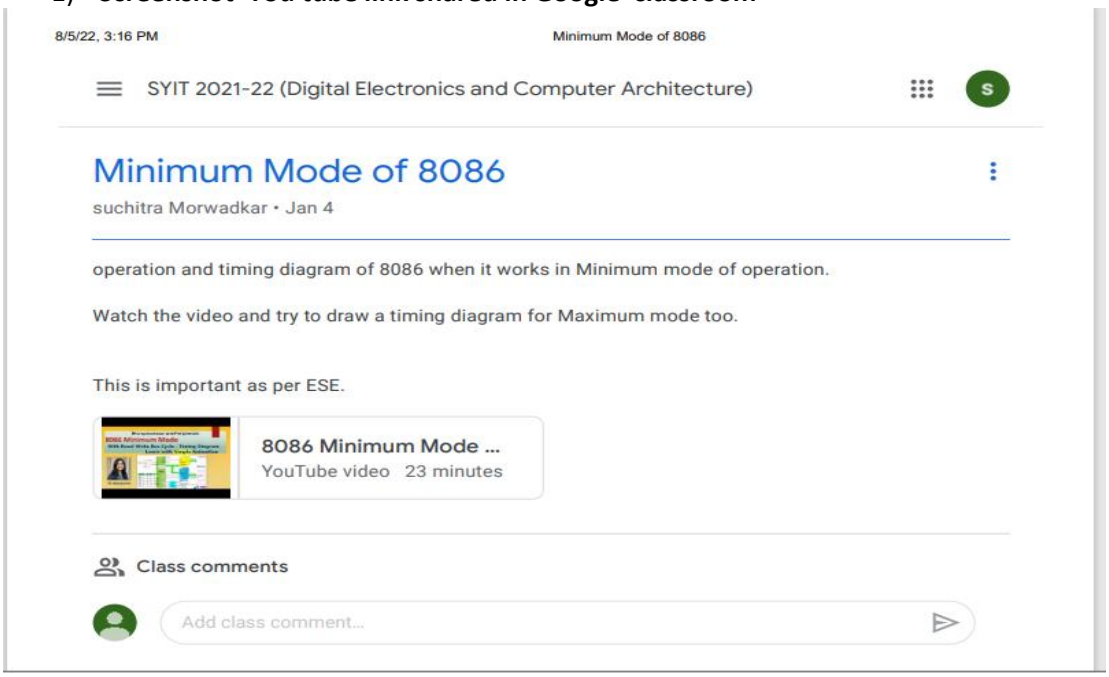
Q.1 Draw and explain interfacing of 8086 when it works in Minimum mode and explain the timing diagram for it.
Q.2 Draw and explain interfacing of 8086 when it works in Maximum mode and explain the timing diagram for it.

The students were expected to upload answers for the assignment in the Google classroom.

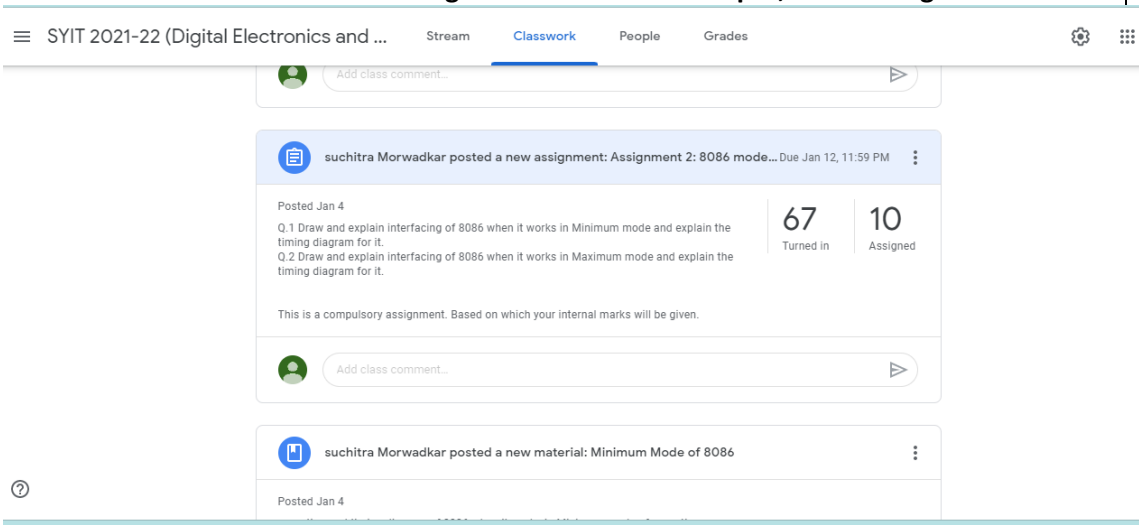
Objective: The objective was to make sure students can draw timing diagrams for various operations of the microprocessor and understand basic difference between read and write cycle.

Impact: Students realised once they understood timing diagram drawing and interpretation for one microprocessor, they can understand and draw the same for any other microprocessor too. Students liked this new way of learning. . They found this technique interesting, helpful, innovative, refreshing, and creative.

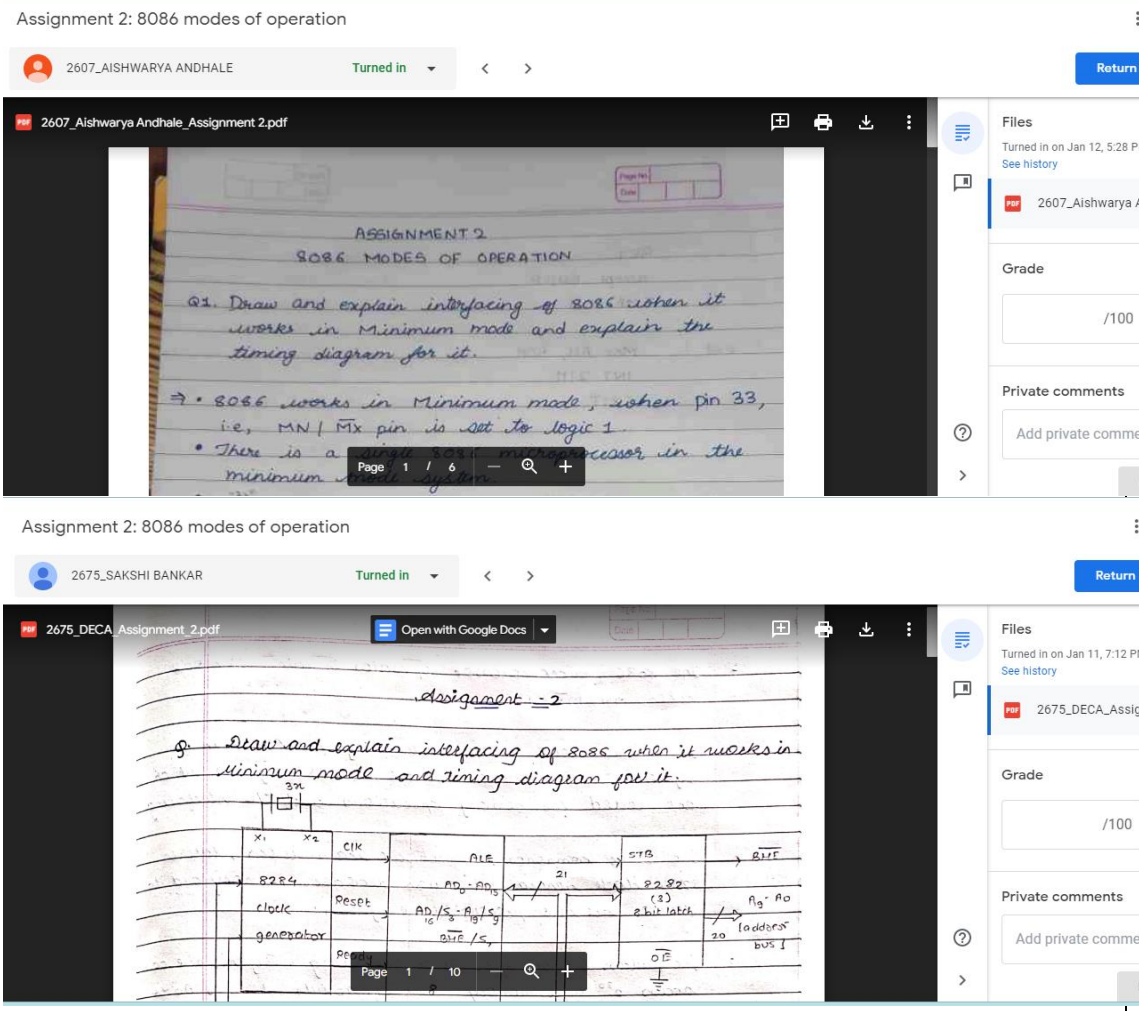
1) **Screenshot You tube link shared in Google classroom**



2) Screen shot of declaration of an Assignment based on the topic , in the Google classroom



3) Screen shots of sample responses uploaded in the Google classroom



4) Sample answer sheet which contains an explanation and timing diagram for Minimum and Maximum modes of 8086

ASSIGNMENT 2

8086 MODES OF OPERATION

Q1. Draw and explain interfacing of 8086 when it works in Minimum mode and explain the timing diagram for it.

⇒ • 8086 works in Minimum mode, when pin 33, i.e, MN / $\overline{MX}$ pin is set to logic 1.

• There is a single 8086 microprocessor in the minimum mode system.

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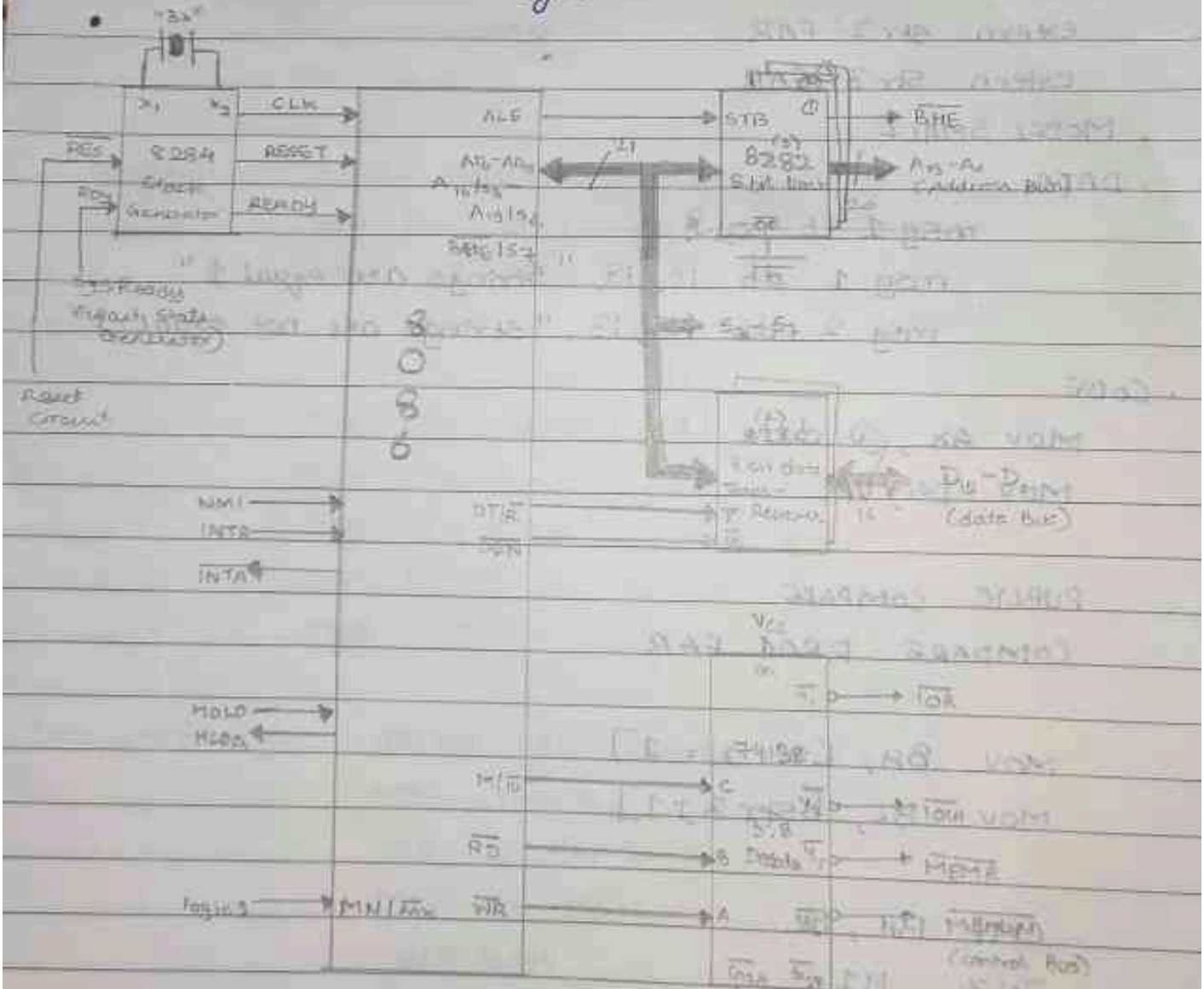


- Clock is provided by 8284 clock generator, it provides CLK, RESET, READY input to 8086.
- Address from address bus is latched into 8282 8-bit latch. We require 3 such latches as the address bus is 20 bit ($3 \times 8 = 24$).
- The ALE of 8086 is connected to STB of the latch.
- The data bus is driven through 8286 8-bit trans-reciever. We require 2 such trans-recievers as the data bus is 16 bit ($2 \times 8 = 16$).
- The trans-reciever is enabled through $\overline{DEN}$ signal, and direction of data is controlled by DT/$\overline{R}$ signal.
- $\overline{DEN}$ is connected to $\overline{OE}$, and DT/$\overline{R}$ is connected to T.

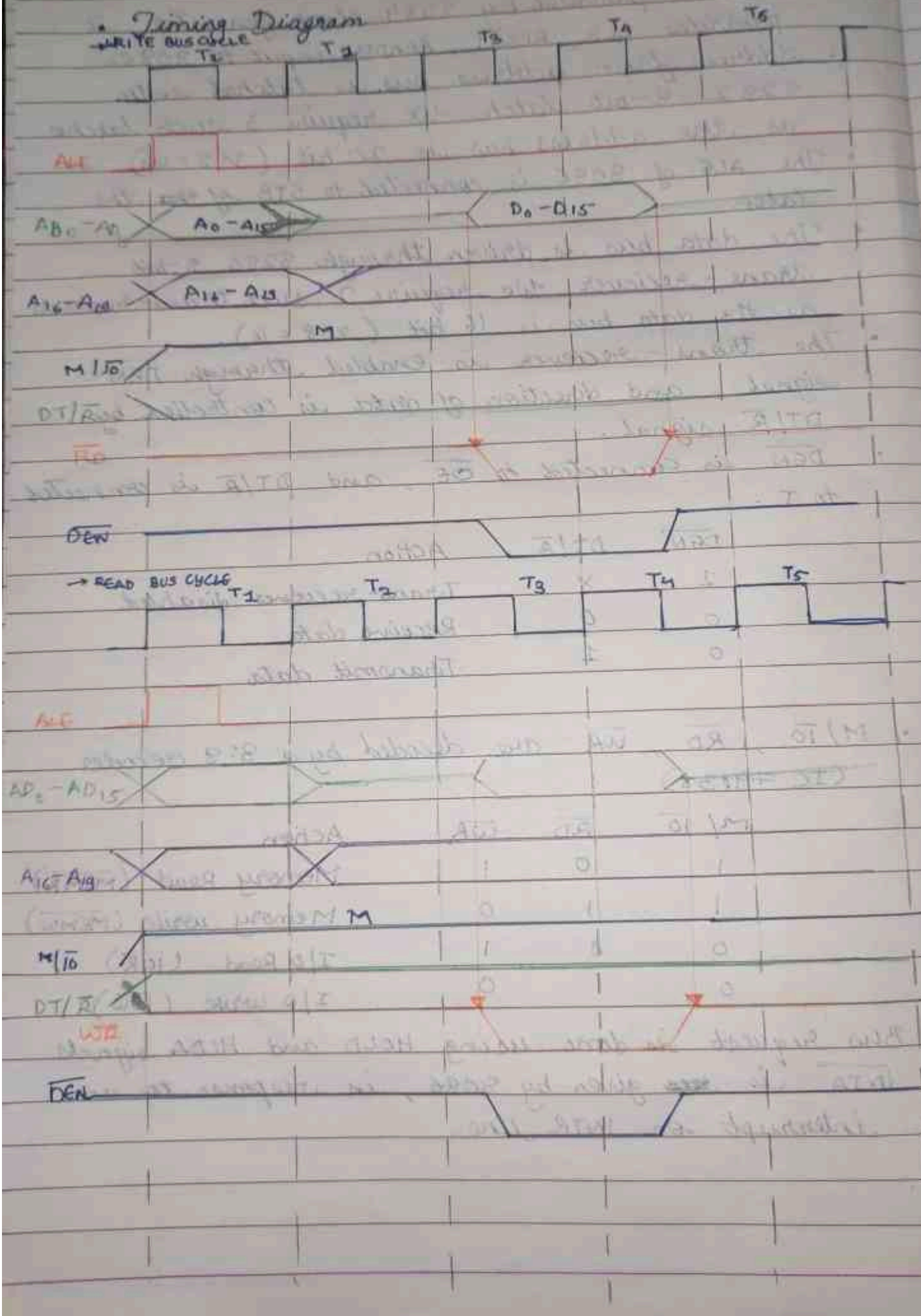
$\overline{DEN}$	DT/$\overline{R}$	Action
1	X	Trans-reciever disabled
0	0	Receive data
0	1	Transmit data

- M/$\overline{IO}$, $\overline{RD}$, $\overline{WR}$ are decoded by a 3:8 decoder (IC 74138)

M/$\overline{IO}$	$\overline{RD}$	$\overline{WR}$	Action
1	0	1	Memory Read ($\overline{MEMR}$)
1	1	0	Memory write ($\overline{MEMW}$)
0	0	1	I/O Read ($\overline{IOR}$)
0	1	0	I/O write ($\overline{IOW}$)

- Bus request is done using HOLD and HLDA signals
- $\overline{INTA}$ is given by 8086, in response to an interrupt on INTR line.

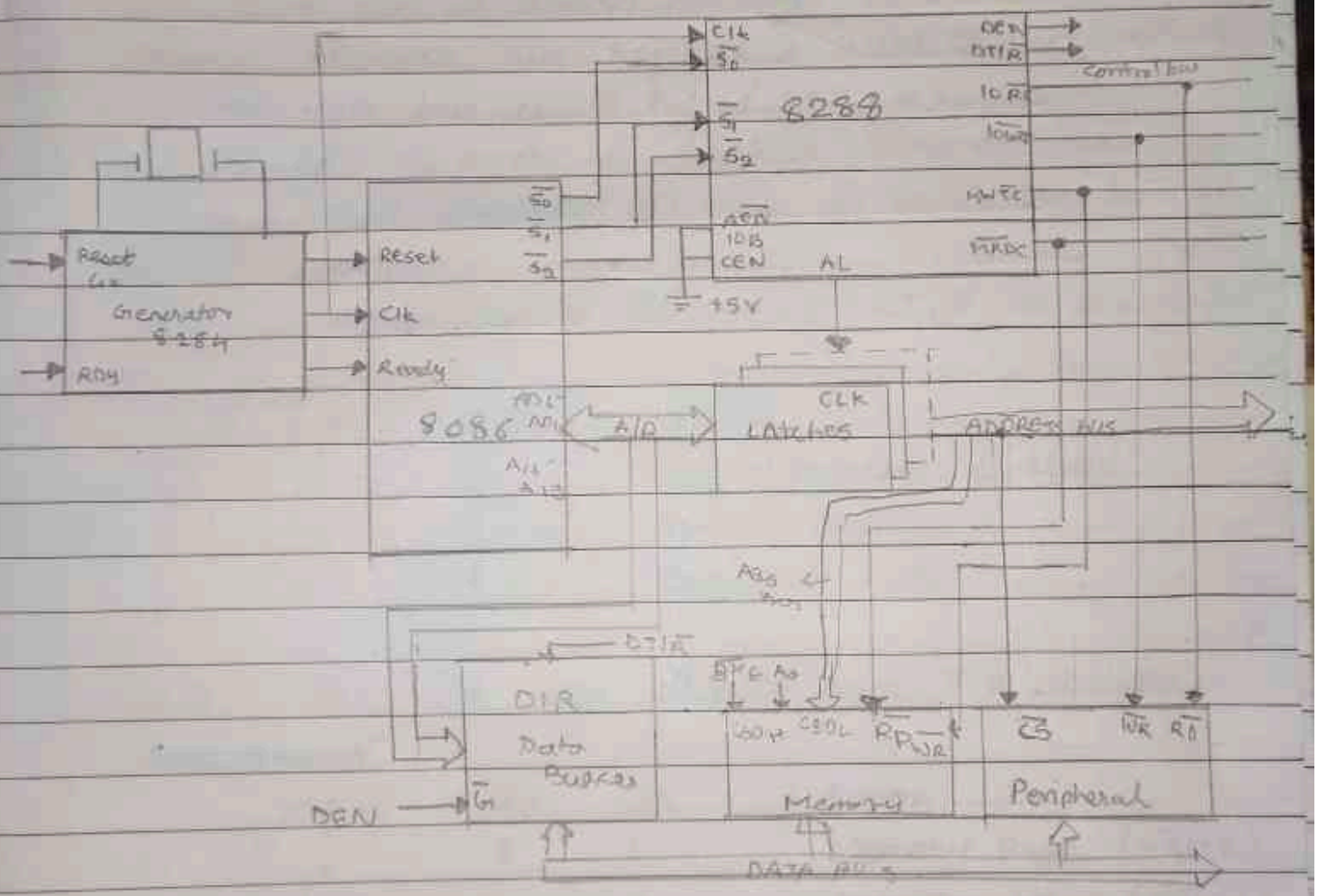
• Timing Diagram



Q2. Draw and explain interfacing of 8086 when it works in Maximum mode and explain the timing diagram for it.

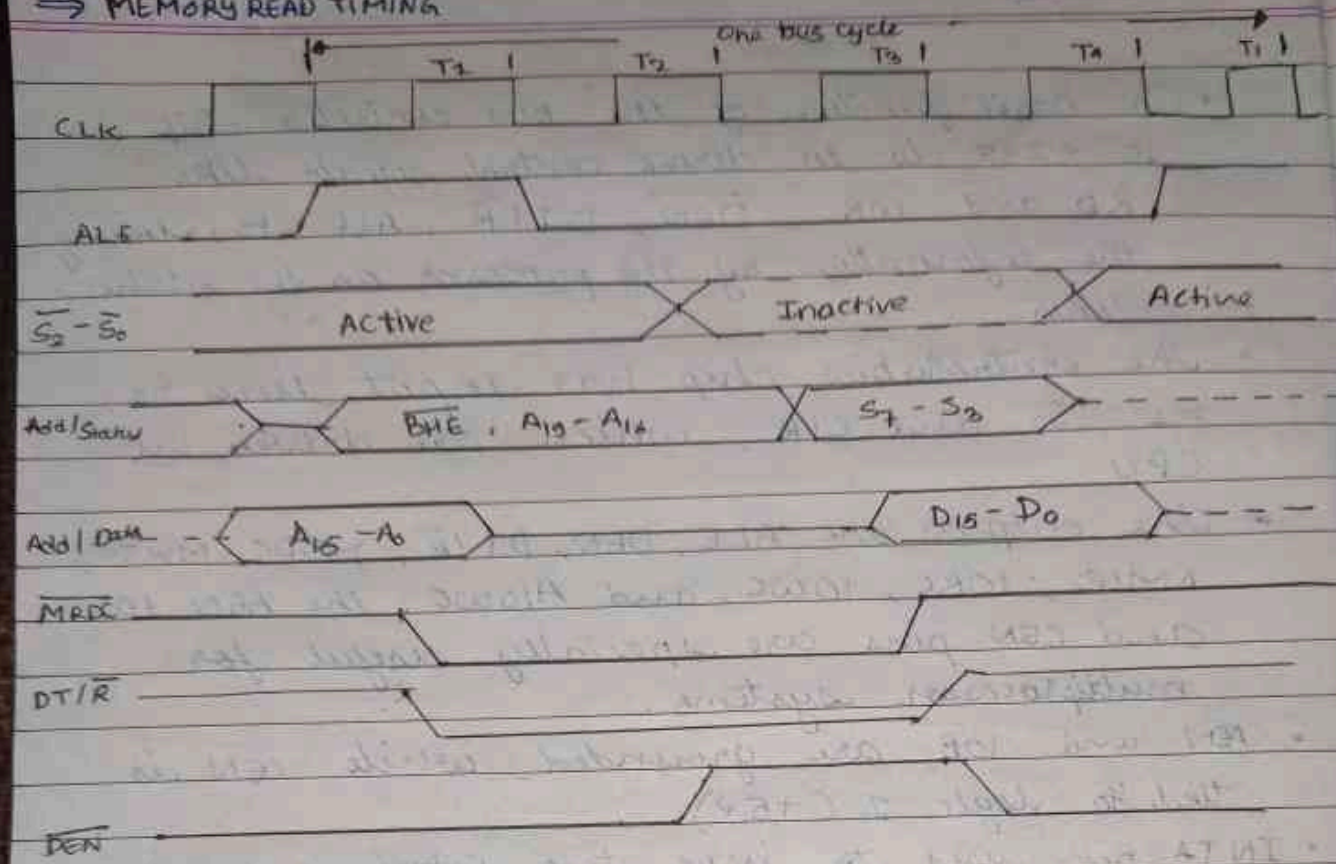
⇒ • 8086 works in Maximum mode, when pin 33, i.e, MN/$\overline{MX}$ pin is set to GND

• In maximum mode, there may be more than one microprocessor in the system configuration



- The basic function of the bus controller chip IC 8288 is to derive control signals like RD and WR, $\overline{DEN}$, DT/$\overline{R}$, ALE etc, using the information by the processor on the status lines.
- The controller bus chip has input lines S_2, S_1, S_0 and Clk, which are driven by CPU
- The outputs are ALE, DEN, DT/$\overline{R}$, MRDC, MWTC, AMWC, IORC, IOWC, and AIOWC. The AEN, IOB and CEN pins are specially useful for multiprocessor systems.
- AEN and IOB are grounded, while CEN is tied to logic 1 (+5 v).
- INTA pin used to issue two interrupt acknowledge pulses to the interrupt controller or to an interrupt device.
- IORC → I/O read command
  IOWC → I/O write command
  These signals enable an I/O interface to read or write data from or to the address port
- MRDC → memory read command
  MWTC → memory write command
  These signals are used as memory read or write signals.

⇒ MEMORY READ TIMING



⇒ MEMORY WRITE TIMING